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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,198	07/20/2005	Leon Maria Albertus Van De Logt	NL 020601	2711

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EXAMINER	
ISLA RODAS, RICHARD	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/520,198	VAN DE LOGT ET AL.	
	Examiner	Art Unit	
	Richard Isla-Rodas	2829	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-8* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 03/29/2006. These drawings are accepted.

Response to Amendment

2. The applicant is reminded that the statement *"No arguments are waived and none of the Examiner's statements are conceded"* is not sufficient to overcome the rejections based on the prior are cited. Therefore, the prior art used to reject the claims in the Non-Final office action remains valid.

Claim Objections

3. Claim 6 is objected to because of the following informalities:

After reading the specification and reviewing the drawings submitted, it isn't clear what the applicant means by ***a further electronic circuit connected with the further electronic circuit***. Therefore for the purpose of examination, the words ***connected with the further electronic circuit*** in the limitation, will be ignored. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to De Jong et al. (6,622,108) in view of the US Patent to Chou (6,591,384).

In terms of claim 1, De Jong et al. show in Figures 4 and 6, an electronic circuit (402) comprising a plurality of input/output (I/O) nodes (nodes for i1, i2, i3, o1, o2) for connecting the electronic circuit to a further electronic circuit (210), a test unit (406) comprising a combinatorial circuit (602) having a plurality of inputs (i1, i2, i3) and an output (o1), the combinatorial circuit implementing an exclusive logic function, the I/O nodes being logically connected (See column 1, lines 22-25) to the test unit in the test mode, wherein a first selection of the I/O nodes (nodes for i1, i2, i3) is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit (602), and a second selection of the I/O node (o1, o2) comprising a first I/O node (o1) and is arranged to carry respective output signals, the first I/O node (o1) coupled to the output of the combinatorial circuit (602), the second selection of the I/O nodes (o1,o2) further comprises a second I/O node (o2) that is coupled to an I/O node (i3) from the first selection of the I/O nodes (i1, i2, i3) in the test mode via a connection (604). De Jong et al. disclose the claimed invention except that the drawings do not

include an inverter in the connection (604). However, it is well known in the art, that XOR gates (element 604 used by Jong to bypass the combinatorial circuit) include at least one inverter as shown by Tsujihashi. Tsujihashi teaches in Figure 4, a XOR gate, similar to that used by De Jong et al. in order to bypass the combinatorial circuit. Said XOR gate includes an inverter (inv1). Therefore, because these two XOR gates were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the XOR gate in De Jong et al. for the XOR gate in Tsujihashi.

As to claim 4, De Jong et al. teach that an alternative is to provide the test circuit with a dedicated test control node, in addition to the I/O nodes, to control whether the circuit is to behave in the normal operational mode or in the test mode (See column 8, lines 35-38).

As to claim 5, De Jong et al. show in Figure 4, a main unit (404) which is logically connected to the I/O nodes (See column 1, lines 22-25), in a functional mode of the electronic circuit, the main unit being arranged to bring the electronic circuit into the test mode upon receipt of a test control signal in a form of a predefined bit pattern through at least a subset of the first selection of I/O nodes (See column 9, lines 61-67).

As to claim 6, in addition to that stated with regards to claim 4, De Jong et al. show in Figure 4, an electronic circuit (402) as claimed in claim 4 and a further electronic circuit (210), wherein the further electronic circuit (210) is arranged to provide the electronic circuit with the test control signal (408) and to provide the first selection of I/O nodes with test patterns for testing the electronic circuit (See column 9, lines 64-65).

As to claim 7, in addition to that stated with regards to claim 6, De Jong et al. show in Figure 4, the further electronic circuit (210) is arranged to receive test result data (through 1:m) from the second selection of I/O nodes.

In terms of claim 8, De Jong et al. teach through Figures 4 and 6, an method for testing an electronic circuit and a further electronic circuit (210), the electronic circuit (402) comprising a plurality of input/output (I/O) nodes (nodes for i1, i2, i3) for connecting the electronic circuit to a further electronic circuit (210), a test unit (406) comprising a combinatorial circuit (602) having a plurality of inputs (nodes for i1, i2, i3) and an output (o1), the combinatorial circuit implementing an exclusive logic function, the I/O nodes being logically connected (See column 1, lines 22-25) to the test unit in the test mode, wherein a first selection of the I/O nodes (nodes for i1, i2, i3) is arranged to carry respective input signals and is connected to the plurality of inputs of the combinatorial circuit (602), and a second selection of the I/O node (o1, o2) comprising a first I/O node (o1) and is arranged to carry respective output signals, the first I/O node (o1) coupled to the output of the combinatorial circuit (602), characterized in that the second selection of the I/O nodes (o1,o2) further comprises a second I/O node (o2) that is coupled to an I/O node (i3) from the first selection of the I/O nodes in the test mode via a connection (604) that bypasses the combinatorial circuit (602) and the method further comprising the act of logically connecting the test unit to the electronic circuit (See column 1, lines 22-25), putting test data on the electronic circuit by the further electronic circuit (See column 9, lines 64-65), and receiving test result data (using lines 1:m) through the first I/O node (nodes for i1, i2, i3) and receiving further test

result data through a second I/O node (o2) that is coupled to an I/O node (i3) from the first selection of the I/O nodes (i1, i2, i3) in the test mode via a connection (604). De Jong et al. disclose the claimed invention except that the drawings do not include an inverter in the connection (604). However, it is well known in the art, that XOR gates (element 604 used by Jong to bypass the combinatorial circuit) include at least one inverter as shown by Tsujihashi. Tsujihashi teaches in Figure 4, a XOR gate, similar to that used by De Jong et al. in order to bypass the combinatorial circuit. Said XOR gate includes an inverter (inv1). Therefore, because these two XOR gates were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the XOR gate in De Jong et al. for the XOR gate in Tsujihashi.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to De Jong et al. (6,622,108) in view of the US Patent to Chou (6,591,384).

In terms of claim 2, De Jong et al. teach all the claimed elements as disclosed above, except for the second selection of I/O nodes further comprising a third I/O node being coupled to a further I/O node from the first selection of I/O nodes in the test mode via a further connection that bypasses the combinatorial circuit. Chou, drawn to circuits for parallel testing of DRAM devices, teaches in Figure 3 and 4B, an electronic circuit (100A), connected to a test unit (340A), the test unit comprising a combinatorial circuit (306, 308) implementing an exclusive logic function, a first selection of the I/O nodes is arranged to carry respective input signals and is connected to the plurality of inputs of

the combinatorial circuit (A'B'C'D'), and a second selection of I/O nodes (IO_0, IO_1, IO_2), comprising a first I/O node (IO_0) arranged to carry respective output signals, the first I/O node (IO_0) being coupled to the output of the combinatorial circuit. The circuit is characterized in that the second selection of the I/O nodes further comprises a second I/O node (IO_1) that is coupled to an I/O node from the first selection of the I/O nodes via a connection (102A) that bypasses the combinatorial circuit. The second selection of I/O nodes (IO_0, IO_1, IO_2), further comprises a third I/O node (IO_2) being coupled to a further I/O node from the first selection of I/O nodes via a further connection (102A) that bypasses the combinatorial circuit. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use the teaching of a second node bypassing a combinatorial circuit as taught by Chou, to include a second node bypassing the combinatorial circuit in De Jong et al. device, in order to allow an additional bit for comparing to the output of the combinatorial circuit and thus increasing accuracy in the testing process.

Allowable Subject Matter

7. Claim 3 is allowed.

The prior art of record does not teach alone or in combination, a second I/O node couple to a buffer and the third I/O node couple to an inverter in combination with all the elements in claim 3.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent to Chou (6,591,384) and Lee (4,575,648).

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Isla-Rodas whose telephone number is (571) 272-5056. The examiner can normally be reached on Monday through Friday 8 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard Isla-Rodas

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04/19/06